ELIZADE UNIVERSITY ILARA MOKIN, ONDO STATE

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

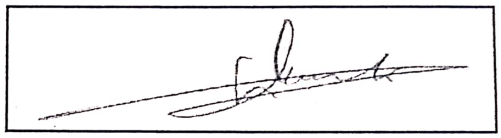
SECOND SEMESTER EXAMINATION, 2017/2018 ACADEMIC SESSION

COURSE TITLE: ELECTRONIC CIRCUIT II

COURSE CODE: EEE 322

EXAMINATION DATE: 1ST AUGUST 2018

COURSE LECTURER: DR K. O. TEMIKOTAN



HOD's Signature

TIME ALLOWED: 2 HOURS 30 MINUTES

INSTRUCTION

1. **ANSWER ALL QUESTIONS IN SECTION A AND FOUR QUESTIONS IN SECTION *B***
2. SEVERE PENALTIES APPLY FOR MISCONDUCT, CHEATING, POSSESSION OF UNAUTHORIZED MATERIALS DURING EXAM.
3. YOU ARE NOT ALLOWED TO BORROW ANY WRITING MATERIALS DURING THE EXAMINATION.

SECTION A

ANSWER ALL QUESTIONS IN THIS SECTION

i. When is a 4-bit sum invalid in a BCD addition?

_____

ii. Convert 11011 in Gray to binary.

_____

iii. Which of these is not an alphanumeric code? (ASCII, Unicode, BCD, EBCDIC)

iv. A NOT gate has $V_{IL} = 0.8$ V, $V_{IH} = 2.5$ V, $V_{OL} = 0.4$ V, and $V_{OH} = 3.6$ V. If two such gates are cascaded, find the high and low margins. Low noise margin is _____ and high noise margin is _____.

v. In a sum of product logic circuit, the output gate is an _____ gate, while in a product of sum logic circuit, the output gate is an _____ gate.

vi. The term fan-in means

_____

_____

_____ **(2 Marks)**

vii. How many flip flops are required to divide a frequency by 32? _____

viii. A counter has n flip flops, the number of states for the flip flop will be less or equal to _____.

ix. Asynchronous counters are also called _____ counters

x. A _____ is a circuit used to select and route any one of several input signals to a single output.

xi. The main disadvantage of MOS ICs is _____ in comparison with TTL ICs.

xii. If the output of a 2-input gate is defined by $Y = \bar{A}B + A\bar{B}$, the gate is a _____ gate

xiii. What is the next number in the series 0 01 10 11 100 101 _____?

xiv. Any logical circuit can be realized using either _____gate or _____ gate.

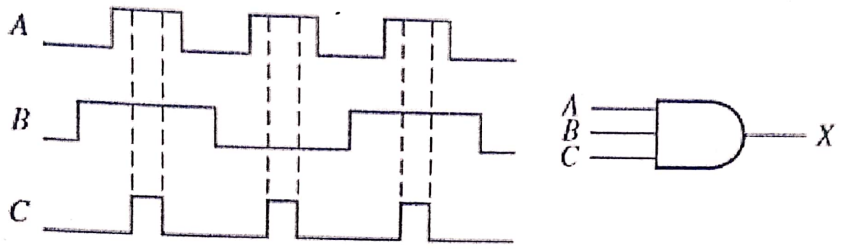
xv. Two functions of a shift register are _____ and _____ **(20 Marks)**

SECTION B

ANSWER ANY FOUR QUESTIONS

QUESTION ONE

a. The input waveforms applied to a 3-input AND gate are as indicated in Figure 1. Show the output waveform represented by X in proper relation to the inputs with a timing diagram.



(2 Marks)

Figure 1 Timing Diagram and Logic Symbol for Question 1

b. Implement $Y = AB + C\overline{D}$ using only NAND gates **(3 Marks)**

c. Design a logic circuit for decimal to BCD encoder. **(5 Marks)**

QUESTION TWO

a. Using Karnaugh map minimize the expression;

$$Z = \bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$$ **(4 Marks)**

b. Design the simplest circuit that has four inputs, A , B, C, and D, which produces an output value of 1 whenever three or more of the input variables have the value of 1; otherwise the output has to be 0. **(6 marks)**

QUESTION THREE

a. Using a diode transistor logic (DTL) design a circuit that can implement;

$X = \overline{(A + \bar{B} + C)}$ **(4 marks)**

b. Draw the Truth Table for the circuit in Figure 2 and derive an expression for F **(6 marks)**

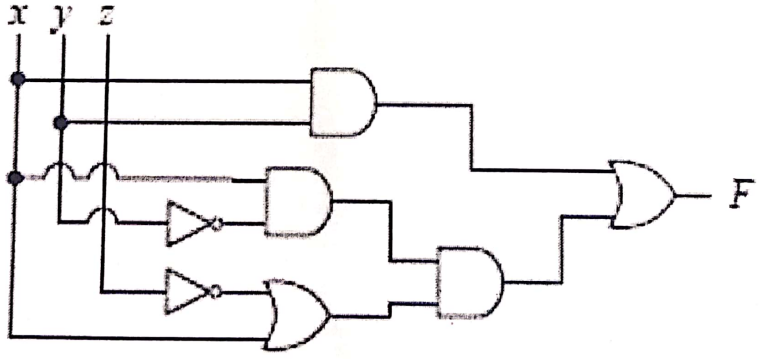


Figure 2 Logic Diagram for Question 3

QUESTION FOUR

a. The min-term of a Boolean expression is given as;

$$Y = (A, B, C) = \sum m(1,3,5,6).$$

Implement this using a multiplexer. **(3 Marks)**

b. Write out the expression for Y and implement using discrete gates. **(3 Marks)**

c. What is a demultiplexer? Given the following truth table for a DEMUX, identify the type and draw the logic circuit for the DEMUX. **(4 Marks)**

Table for Question 3c

A	B	D	A_0	A_1	A_2	A_3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

QUESTION FIVE

a. List and explain briefly five performance characteristics of an analogue to digital converter. 4 marks

b. Draw a 4-bit R/2R ladder DAC and explain its principles of operation. **(4 Marks)**

c. Determine the percentage resolution of the the following digital to analogue converters.

i. An 8-bit DAC

ii. A 16- bit DAC **(2 Marks)**

QUESTION SIX

a. Show how a J K flip flop can be converted to a D flip flop. **(2 Marks)**

b. A counter is required to count the number of bottles being automatically filled in a plant. Each time a bottle crosses an electronic sensor a pulse is generated. If 1000 bottles are to be counted, what is the minimum number of flip flops required? **(2 marks)**

c. Determine the output of the DAC in Figure 3 if the input signal is 1011. D_0 is the least significant bit. Assume that binary 1 represents 5 V. **(6 Marks)**

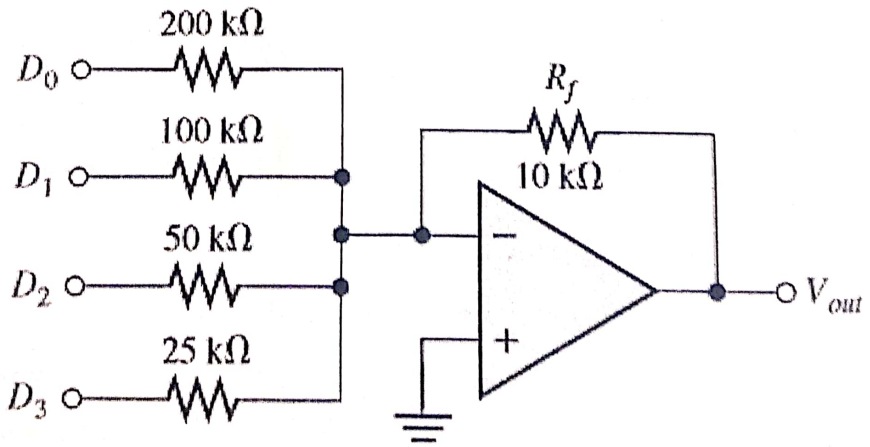


Figure 3. DAC for Question 6c **(6 Marks)**